

FIG. 1

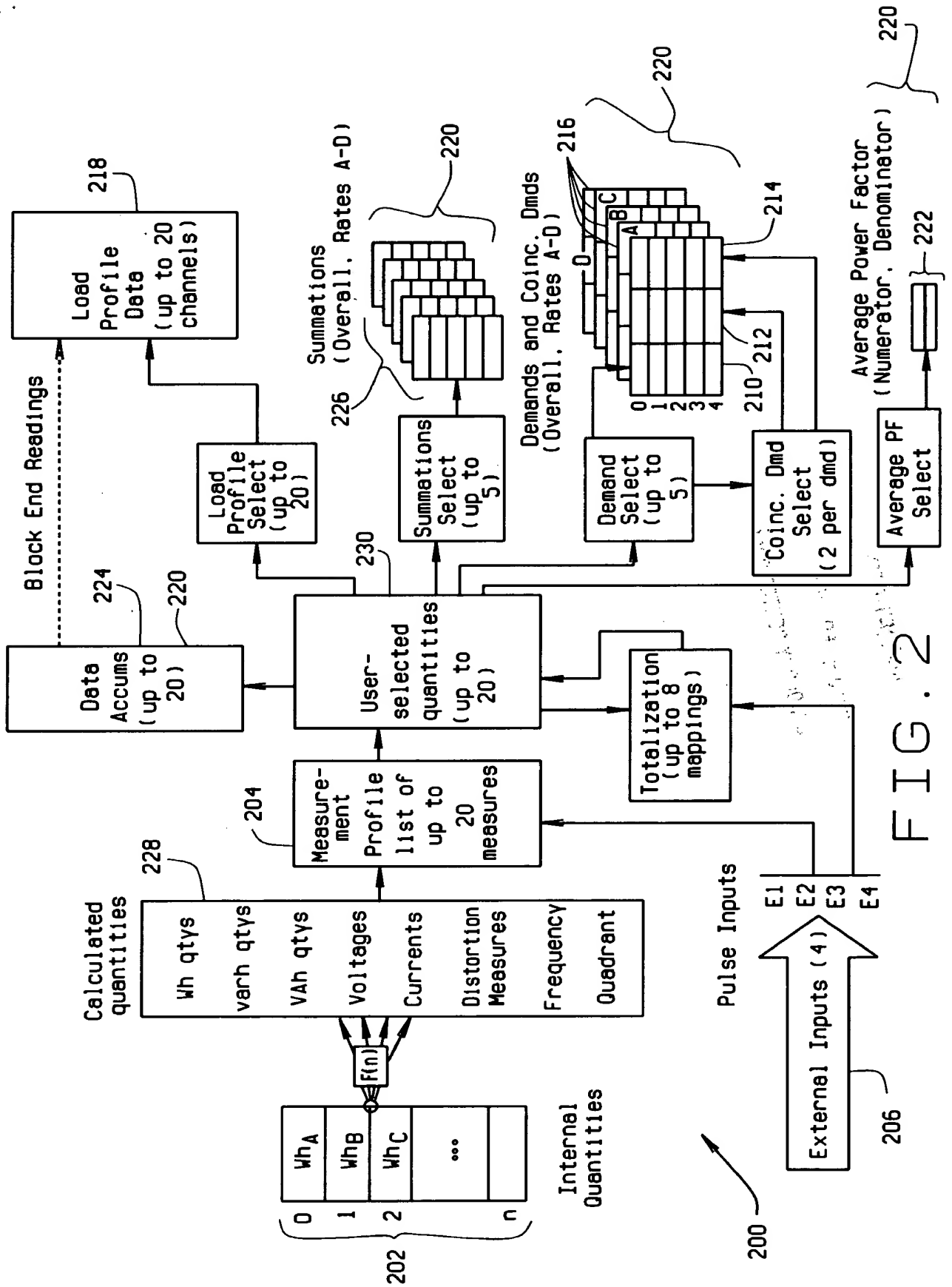
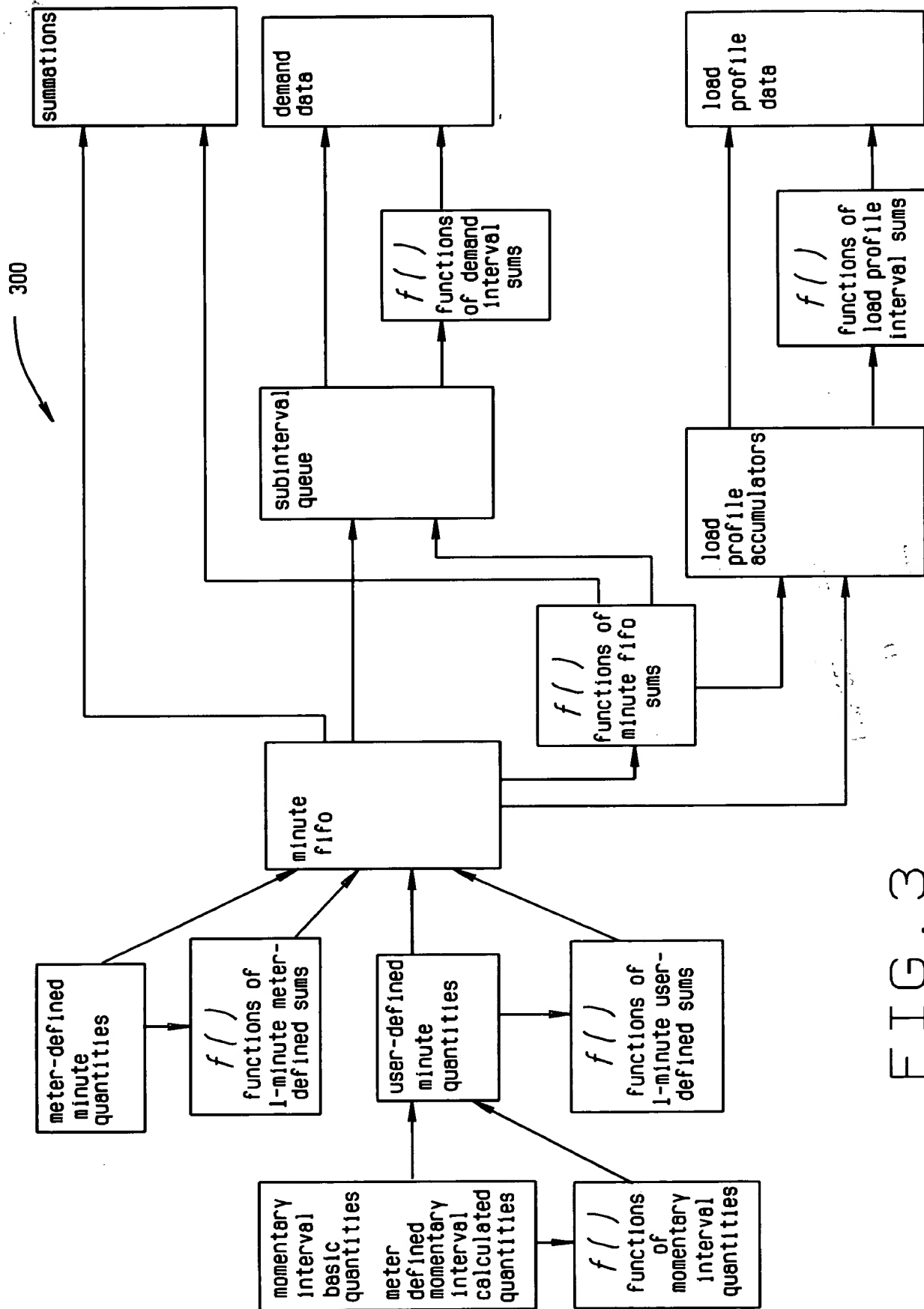


FIG. 2



Signal	Normal Mode	ID Mode	Address Mode	Read Mode	Write Mode
I/O_LATCH	0	1	Hi-to-Lo Transition	0	0
I/O_READ	0	1	0	1	0
I/O_WRITE	0	0	0	0	Hi-to-Lo Transition
I/O_DATA_0	Hi-Z w/Pulldown	Address Bit 0	Address Bit 0	Input Bit 0	Output Bit 0
I/O_DATA_1	Hi-Z w/Pulldown	Address Bit 1	Address Bit 1	Input Bit 1	Output Bit 1
I/O_DATA_2	Hi-Z w/Pulldown	Address Bit 2	Address Bit 2	Input Bit 2	Output Bit 2
I/O_DATA_3	Hi-Z w/Pulldown	Response Bit 0	Sub-Address Bit 0	Input Bit 3	Output Bit 3
I/O_DATA_4	Hi-Z w/Pulldown	Response Bit 1	Sub-Address Bit 1	Lo-/Hi Nibble	Lo-/Hi Nibble

FIG. 4

Signal	ID Mode	Address Mode	Read Mode	Write Mode(Nib 0)
I/O_LATCH	1	Hi-to-Lo Transition	0	0
I/O_READ	1	0	1	0
I/O_WRITE	0	0	0	Hi-to-Lo Transition
I/O_DATA_0	1	1	N/A	KYZ 1 Output
I/O_DATA_1	0	0	N/A	KYZ 2 Output
I/O_DATA_2	0	0	N/A	Switch 1 Output
I/O_DATA_3	1	X	N/A	N/A
I/O_DATA_4	0	X	N/A	0

FIG. 5

APPROVED	O.G. FIG.	
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Signal	ID Mode	Address Mode	Read Mode(Nib 0)	Read Mode(Nib 1)	Write Mode(Nib 0)	Write Mode(Nib 1)
I/O_LATCH	1	H1-to-Lo Transition	0	0	0	0
I/O_READ	1	0	1	1	0	0
I/O_WRITE	0	0	0	0	H1-to-Lo Transition	H1-to-Lo Transition
I/O_DATA_0	1	1	Z1 Input	Z3 Input	KYZ 1 Output	Switch 3 Output
I/O_DATA_1	0	0	Y1 Input	Y3 Input	KYZ 2 Output	Switch 4 Output
I/O_DATA_2	0	0	Z2 Input	Z4 Input	Switch 1 Output	Switch 5 Output
I/O_DATA_3	0	X	Y2 Input	Y4 Input	Switch 2 Output	Switch 6 Output
I/O_DATA_4	1	X	0	1	0	1

FIG. 6

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